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(54) **Polycrystalline semiconductor resistor**

(57) Reduction in 1/f noise is obtained in polycrystalline semiconductor material resistors having a common interface with insulating material 16, 18 by profiled implantation of impurity ions so that the impurity concentration in the interior region 22a' of the resistor is higher relative to the impurity concentration near the boundary 22g, 22h, of the resistor. Such a profiled implantation channels the charge carrier current flow through the resistor away from the interface between the polycrystalline material and the insulating material thus reducing surface state noise.

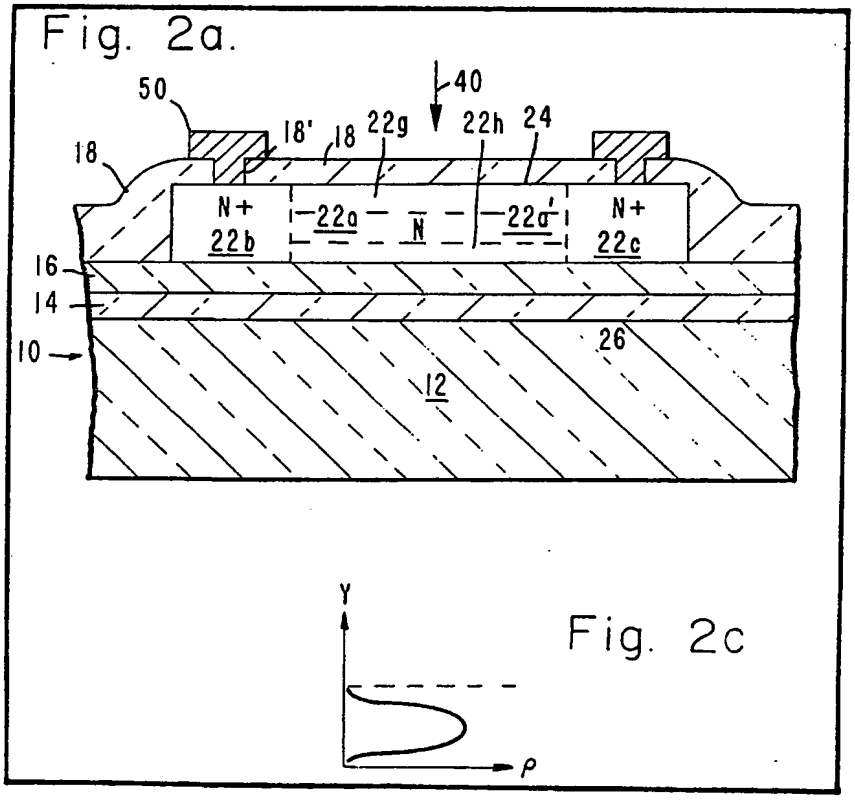

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Fig. 1.

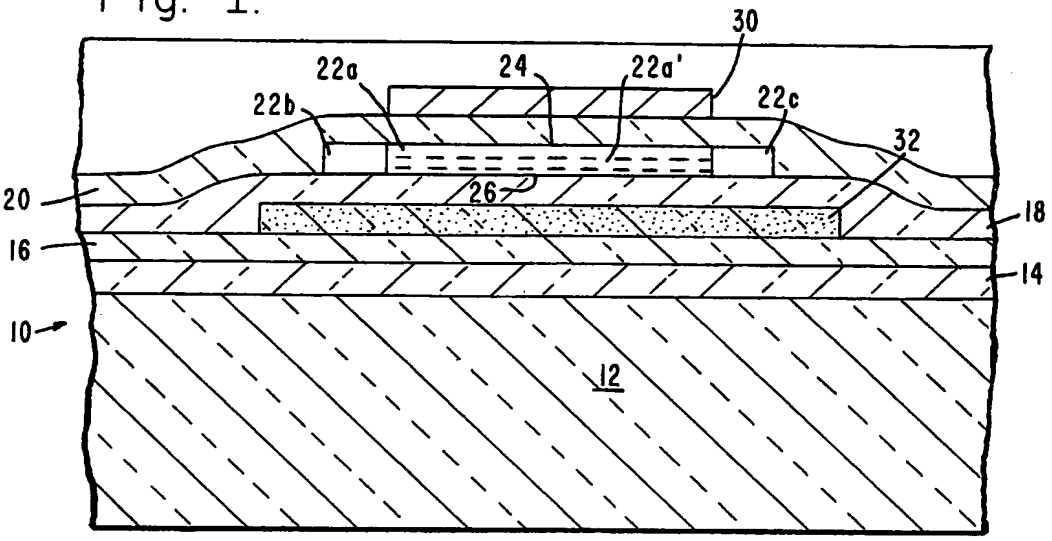


Fig. 2b.

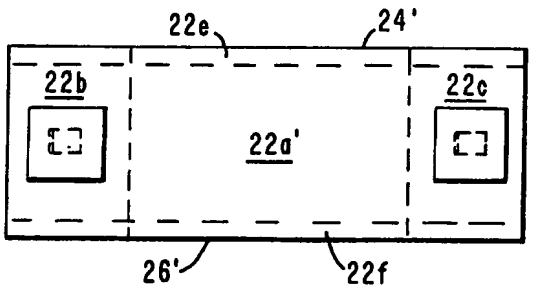


Fig. 2d.

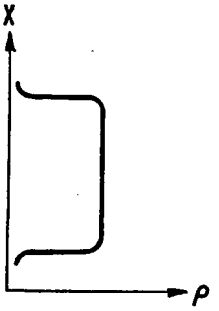


Fig. 2a.

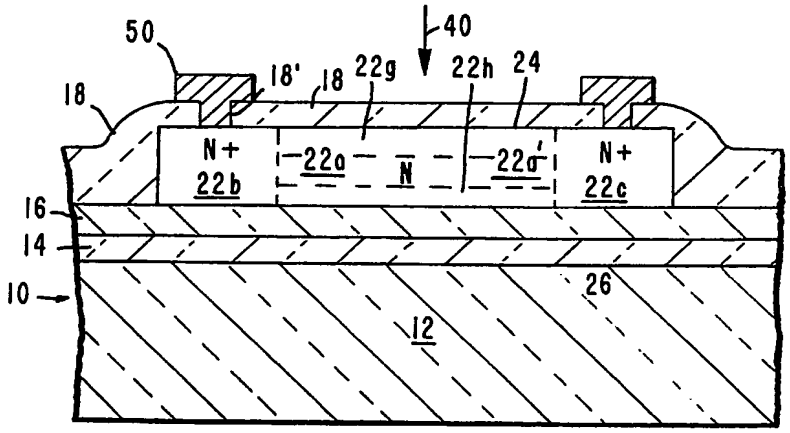
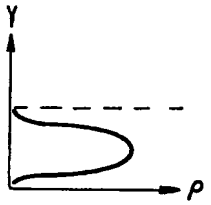


Fig. 2c



SPECIFICATION

Polycrystalline semiconductor resistor with profiled ion implantation for reducing noise

Technical field

This invention is related to techniques for reducing I/f noise in polycrystalline silicon resistors used in metal oxide semiconductor (MOS) circuits such as imagers and random access memories.

Background art

A significant advance in metal oxide semiconductor (MOS) technology was the introduction of polycrystalline silicon resistors which are formed in a dielectric layer overlying the silicon substrate. A polycrystalline silicon resistor comprises a strip of polycrystalline silicon formed in the dielectric layer overlying the substrate, the resistivity of the polycrystalline resistor being determined by the concentration of implanted doping impurities. By using ion implantation, the resistivity may be selected with great accuracy, a significant advantage. Furthermore, the polycrystalline resistor does not take up room on the underlying substrate, which improves device density on the integrated circuit.

One problem with polycrystalline silicon resistors is that transmission of a signal through a polycrystalline silicon resistor introduces noise into that signal which is inversely proportional to the frequency. This type of noise is commonly called I/f noise. It is believed that this noise arises from the presence of surface states at the interface between the polycrystalline silicon resistor and the surrounding dielectric layer. The phenomenon of surface state noise is well known in the art. Polycrystalline silicon germanium has been studied by Chin, "Electrical and Noise Properties of Vacuum Deposited Thin Germanium Films", PhD Thesis, University of South Florida, 1976. Such noise is a significant problem if the polycrystalline semiconductor resistor is to be used as a photodetector load resistor in a charge coupled device imager array, because such noise degrades the quality of the image produced by the imager. Such noise is also a significant problem if the polycrystalline semiconductor resistor is to be used in a semiconductor memory such as a random access memory formed on an integrated circuit substrate, inasmuch as the I/f noise can introduce errors into the memory. Accordingly, it has been a goal in the art to somehow eliminate or at least reduce I/f noise in polycrystalline semiconductor resistors.

Summary of the invention

In the present invention, I/f noise in a polycrystalline silicon resistor is reduced by confining current flow through the polycrystalline semiconductor resistor in a central region away from the boundaries between the polycrystalline semiconductor resistor and the surrounding dielectric layer. The result is that the charge carriers comprising the current flowing through the resistor do not interact with the surface states at the boundaries between the polycrystalline semiconductor resistor and the surrounding dielectric, thus significantly reducing I/f noise.

In the present invention, the preferred embodiment includes a polycrystalline semiconductor resistor surrounded by a dielectric layer overlying a semiconductive substrate. The conductivity of the resistor is increased by profiled ion implantation of dopant impurities into the polycrystalline semiconductor material. The concentration of the impurities is relatively high through the internal center region of the polycrystalline resistor, but is relatively low at the edge boundaries of the resistor. The conductivity of the resistor is thus very high in the center region so that current flow is confined therein away from the edge boundaries of the resistor.

Description of the drawings

The invention is best understood by reference to the accompanying drawings, of which:

Fig. 1 is a simplified cross-sectional view of a polycrystalline resistor;

Fig. 2a is a simplified cross-sectional view of an integrated circuit illustrating the technique of the present invention for reducing noise in polycrystalline semiconductor resistors using profiled ion implantation;

Fig. 2b is a plan view corresponding to Fig. 2a;

Fig. 2c illustrates the implanted dopant density distribution in the resistor corresponding to the cross-sectional view of Fig. 2a; and

Fig. 2d illustrates the implanted dopant density distribution in the resistor corresponding to the plan view of Fig. 2b.

Detailed description of the invention

Fig. 1 illustrates an integrated circuit 10 including a semiconductive silicon substrate 12 and overlying dielectric layers 14, 16, 18 and 20 comprising silicon dioxide. A polycrystalline silicon resistor 22 is surrounded by the dielectric layers 18 and 20 and overlies the silicon substrate 12. The resistor 22 is preferably formed by lightly implanting donor-type dopants (for example, arsenic) in a middle resistor portion 22a and heavily implanting donor-type dopants in contact portions 22b, 22c at either end of the resistor 22.

Figs. 2a and 2b illustrate an exemplary polycrystalline silicon resistor structure wherein the overlying dielectric layer 18 has contact holes 18' formed therein through which metal contacts 50 may be formed to each of the heavily doped contact ends 22b, c of the resistor 22. Electrons introduced at one of the ends 22b, 22c flow through the resistor portion 22a to the opposite end.

The problem with the resistor 22 is that surface states, comprising lattice imperfections or empty atomic sites, are present at the top boundary 24 and the bottom boundary 26 and all other boundaries between the resistor 22 and the

surrounding oxide layers 18, 20. Electrons flowing through the resistor 22 interact with the surface states, which introduces noise into the signal represented by the electron current. This noise is inversely proportional to the frequency and is commonly called l/f noise.

This problem is solved by the introduction of a field plate facing the resistor 22, the field plate introducing an electric field near one of the boundaries 24, 26 so that carriers flowing between the two ends 22b, 22c of the resistor 22 are forced away from the boundary. This reduces the electron and surface state interaction and therefore reduces l/f noise.

One field plate may be an aluminum field plate 30 (Fig. 1) formed over the dielectric layer 20 and overlying the polycrystalline silicon resistor 22. Another field plate may be a polycrystalline silicon field plate 32 formed beneath the resistor 22 between the dielectric layers 16, 18. The polycrystalline field plate 32 is heavily doped with, for example, donor-type impurities using well-known techniques so that the polycrystalline material in the field plate 32 is virtually conductive. If a negative potential is applied to the aluminum field plate 30, an electric field will be created which forces electron carriers in the resistor 22 away from the boundary 24. If a negative potential is applied to the polycrystalline field plate 32, an electric field in the opposite direction will be created which repels electron carriers in the resistor 22 away from the bottom boundary 26.

It is preferable to simultaneously repel electron carriers in the resistor 22 from both boundaries 24, 26 by applying negative potentials to both field plates 30, 32. This causes repulsive electric fields to be present at both boundaries 24, 26 so that electron carriers are driven away from the boundaries 24, 26 and confined to a central region 22a' in the interior of the resistor 22, thus reducing the electron and surface state interaction and therefore reducing the l/f noise.

In Figs. 2a and 2b, the polycrystalline silicon resistor 22 is implanted in such a manner that the peripheral portions 22e, f, g, h near the top and bottom boundaries 24, 26 and side boundaries 24', 26' of the resistor 22 are relatively nonconductive in comparison with the central region 22a'. In order to accomplish this, profiled ion implantation is performed on the polycrystalline silicon resistor 22 to create the vertical distribution of implanted dopants illustrated in Fig. 2c (corresponding to the cross-sectional view of Fig. 2a) and the horizontal distribution of implanted dopants illustrated in Fig. 2d (corresponding to the plan view of Fig. 2b).

In order to achieve the vertical distribution of implanted dopants illustrated in Fig. 2c, an ion beam 40 comprising dopant ions (such as an acceptor dopant which may be arsenic ions) is directed toward the top boundary 24. The energy of the beam 40 is precisely selected so that the density ρ of implanted dopant impurities assumes the vertical distribution illustrated in Fig. 2c. This selection, of course, will vary depending upon the particular device geometries involved. Techniques for achieving the distribution illustrated in Fig. 2c are well known in the art of ion implantation and will not be described here. Generally, the peak of the distribution curve illustrated in Fig. 2c should correspond to the vertical center of the central region 22a' of the resistor 22.

The horizontal distribution of dopant impurities illustrated in Fig. 2d is achieved by a suitable mask, such as photoresist, placed over the top surface 24 prior to the ion implantation step of Fig. 2a. The extent of the mask is such that only the central region 22a' is exposed to the implantation beam 40, the peripheral regions 22e, 22f being shielded by the mask. Use of photoresist as an ion implantation mask is a well-known technique in the art and will not be described further herein.

The resistivity of the resistor is inversely proportional to the dopant concentration ρ. Accordingly, the vertical distribution of dopant concentration ρ of Fig. 2c and the horizontal distribution of Fig. 2d makes the peripheral regions 22e, f, g, h relatively nonconductive while the center region 22a' is relatively conductive and has a resistivity determined by the concentration ρ of implanted dopants therein. Accordingly, the resistivity of the resistor 22 may be accurately selected, while at the same time l/f noise may be reduced by the profiled ion implantation characterized by Figs. 2c and 2d. Most of the electrons flowing between the two contact ends 22b, 22c of the resistor 22 flow only through the central region 22a', so that electron interaction with the surface states present at the vertical boundaries 24, 26 and the side boundaries 24', 26' is significantly reduced. As a result, l/f noise in the resistor is reduced proportionately.

Claims

1. An improved polycrystalline resistor, comprising;

a semiconductive substrate;

an overlying dielectric layer on said substrate;

a polycrystalline semiconductor layer formed in said dielectric layer and separated therefrom by a boundary therebetween; and

dopant impurities in said polycrystalline semiconductor layer having a concentration which is relatively low near said boundary and relatively high at an interior region of said polycrystalline semiconductor layer.

2. An improved low noise polycrystalline semiconductor resistor, comprising:

a polycrystalline semiconductor layer surrounded by a dielectric layer forming an interface boundary therebetween; and

dopant impurities in said layer having a density ρ which is reduced near said interface boundary.

3. A method for making a polycrystalline semiconductor resistor, comprising:

forming a polycrystalline semiconductor layer surrounded by a dielectric layer and defining an interface therebetween;

performing profiled ion implantation of dopant impurities into said polycrystalline semiconductor layer whereby implanted dopant concentration is minimized near said boundary.

4. The method of Claim 3 wherein said ion implantation step comprises selecting an ion implantation beam energy whereby a majority of the ions are implanted in an interior portion of said polycrystalline semiconductor layer.

5. The method of Claim 3 wherein said ion implantation performing step comprises forming an ion implantation mask over said polycrystalline semiconductor layer which covers a peripheral region of said polycrystalline semiconductor layer near said boundary and permits implantation into an interior region of said resistor.

6. A low noise polycrystalline semiconductor resistor, comprising:

a semiconductor substrate having an overlying dielectric layer;

a polycrystalline semiconductor resistor, through which a charge carrier current may flow, formed in said dielectric layer; and

means for confining charge flow in said resistor to an interior region thereof, comprising implanted dopant impurities in said resistor having a maximum concentration in said interior region and a lesser concentration elsewhere.

7. A method for making a low noise polycrystalline semiconductor resistor, comprising:

forming a polycrystalline layer defined by at least one boundary adjacent a dielectric layer;

distributing dopant impurities in said polycrystalline layer so that said impurities have a maximum concentration in an interior region of said polycrystalline layer away from said boundary and have a lesser concentration in a peripheral region of said polycrystalline layer near said boundary.

8. The method of Claim 7 wherein said distributing step comprises ion implanting said impurities at a particular implantation energy level, said energy level being selected so that the concentration of implanted impurities is reduced in said peripheral region near said boundary and is maximized in said interior region.

9. A polycrystalline semi-conductor resistor substantially as herein described with reference to Figure 1 or Figures 2*a* and 2*b* of the accompanying drawings.

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